

# HDMI Comparative Trace Impedance Demonstration Boards "B-CMD-HDMI-EVB REV 1"

20050504v02(A, B, C, D, E and F)

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## INTRODUCTION

***WARNING! The sample diagrams in this document ARE NOT INTENDED AS and CANNOT BE USED AS dimensionally accurate recommended reference layouts!! DO NOT ATTEMPT TO CUT-AND-PASTE HARD GERBERS INTO YOUR SYSTEM...IT WON'T WORK!!***

The nature of HDMI TMDS signals requires careful simulation and design of traces and layouts based on numerous variables which may change radically from customer to customer, and especially from PCB vendor to PCB vendor. CMD provides IBIS simulation models for MediaGuard™ devices and can assist the designer with the development of an HDMI compliant design including actual TDR testing of prototype PCBs. However, a successful HDMI implementation cannot be produced by traditional reference design cut-and-paste methods that may have been sufficient in other applications.

The CM2020 and CM2021 MediaGuard™ family of HDMI Interface protection ICs are designed to simplify the layout of HDMI printed circuit boards (PCBs.) This document demonstrates the minute differences in layout that can mean the difference between a failing and passing differential impedance test.

The 0.5mm spacing of the MediaGuard™ interface devices are ideally suited for both surface mount (SMT) and even pin-through-hole (PTH) connectors. The native pin spacing of HDMI connectors is 0.5mm, and this is reflected in the 0.5mm spacing of the PCB pads of the SMT connectors, and is also reflected in the effective 0.5mm spacing of the three-row 1.5mm spacing PTH connectors (1.5mm/3 = 0.5mm).

## TDR MEASUREMENTS

Time Domain Reflectometry (TDR) is the time-domain corollary to a frequency spectrum analyzer. A TDR graph is an interpolated plot of Zo along the transmission line under test.

Therefore, we are seeing discrete points plotted of  $Z = \sqrt{\left(\frac{L}{C}\right)}$  with an averaged line drawn through them.

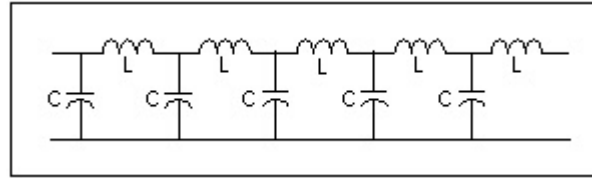


Figure 1 Discrete Simplification of an Ideal T-Line

The output of a TDR oscilloscope can vary widely depending on the setting of the incident risetime of the reference TDR pulse.

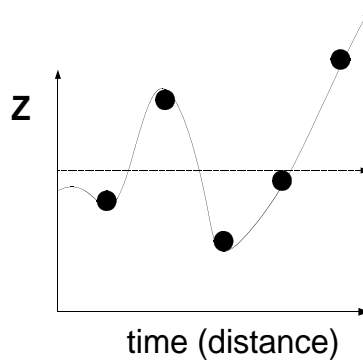


Figure 2 High Resolution TDR Plot (Fast Risetime)

The risetime of the TDR scope obviously does not change the impedance, since L and C along the t-line are set by the PCB and components, however TDR plots are usually "aliased" to an upper frequency bound of interest.

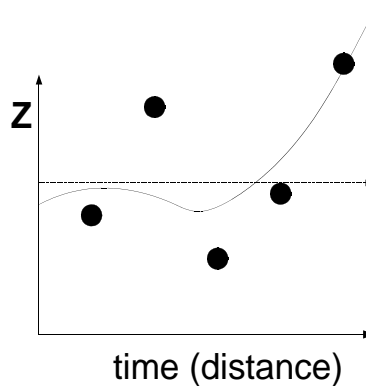


Figure 3 Lower Resolution (Slow Risetime)



The risetime of the TDR scope only sets the resolution of the time domain plot that is being viewed. You can directly see this by looking at the narrowest "peak" of a TDR plot, as this will give you an indication of how narrow the delta-L and delta-C can actually be resolved. At 30ps and with the propagation delay of the MediaGuard demonstration boards, this is the equivalent of about 2mm of resolution...which is about half the width of the MediaGuard™ part.

While any risetime *less than* 200ps can be used to measure the impedance curve for HDMI compliance, using a faster (higher resolution) pulse can show the designer each actual parasitic element of the design for better understanding of problem areas. A longer TDR risetime reduces this resolution and simply averages the nearby traces into the "lumped impedance" described in Q1 of the MediaGuard FAQ.

Actually, most TDR scopes do not have an adjustable risetime! They merely include an averaging math function available to "simulate" slower risetimes by averaging adjacent samples. So when a test quotes a 100ps or 200ps, they are simply lowering the bandwidth and resolution, which does indeed typically have the effect of averaging out the delta-C and delta-L.

The CMD Comparative Trace Impedance Demonstration Boards are designed specifically to compare and contrast different PCB layout configurations and highlight the advantages and disadvantages of each.

There are several layout segments on the boards described in this Evaluation Board Documentation. These are referred herein as "C-MG"-- the distance between the Connector and MediaGuard (determined by the designer...should be around 2-3mm for a nice layout,) "MG-MG"-- the distance underneath the MediaGuard chip (fixed by the width of the TSSOP package), and the "Stub"--- between the MediaGuard chip and the differential pair, with its length also depending on the designer's layout.

These three PCB trace segments have a special function. They are each effectively a pi-filter with a characteristic delta-L and delta-C that is determined by the customer's PCB stackup and fab process. Their length, width, thickness, plating, dielectric thickness and permittivity must be chosen to offset the parasitics described in the MediaGuard IBIS model.

C-MG and MG-MG will be combined by the TDR tester with the parasitics of the MG pins on the connector side of Mediaguard. These PCB arrangements can be "tweaked" and "necked down" and otherwise adjusted to get an average closer to the 100 Ohm target.

A 200ps TDR measurement will combine the MG-MG trace and the "stub" area with the parasitics of the MG pins on the ASIC side of Mediaguard. These PCB arrangements can also be independently "tweaked" and adjusted to get an average closer to the 100 Ohm target.

The CMD Comparative Trace Impedance Demonstration Boards demonstrate many combinations of these adjustments and tweaks and how they affect the outcome at the high resolution shown in our documentation.

By demonstrating these boards at <35ps, designers can see better how minute alterations to different segments (i.e. changing the trace widths from 4.5, to 5.0 to 5.5mils) can affect the actual segmented contribution to overall impedance. Generally, when the differences in TDR peaks and valleys are minimized at the fastest risetime, then the maximum impedance margin will have been achieved for HDMI compliance.

## **DEMONSTRATION BOARD DESCRIPTIONS**

There are six permutations of the 20050504v02 impedance demonstration boards, grouped in two sets.

Three boards are designed with typical Silicon Image HDMI receiver chips (Boards A, B and C) and three are designed with 100 Ohm differential termination resistors (Boards D, E and F.)

These boards are NOT intended as "reference designs." The trace dimensions are intentionally staggered to demonstrate that the same chip can pass or fail TDR testing merely by how the PCB is laid out.

The following 4-layer stackup is common to all six 20050504v02 boards.

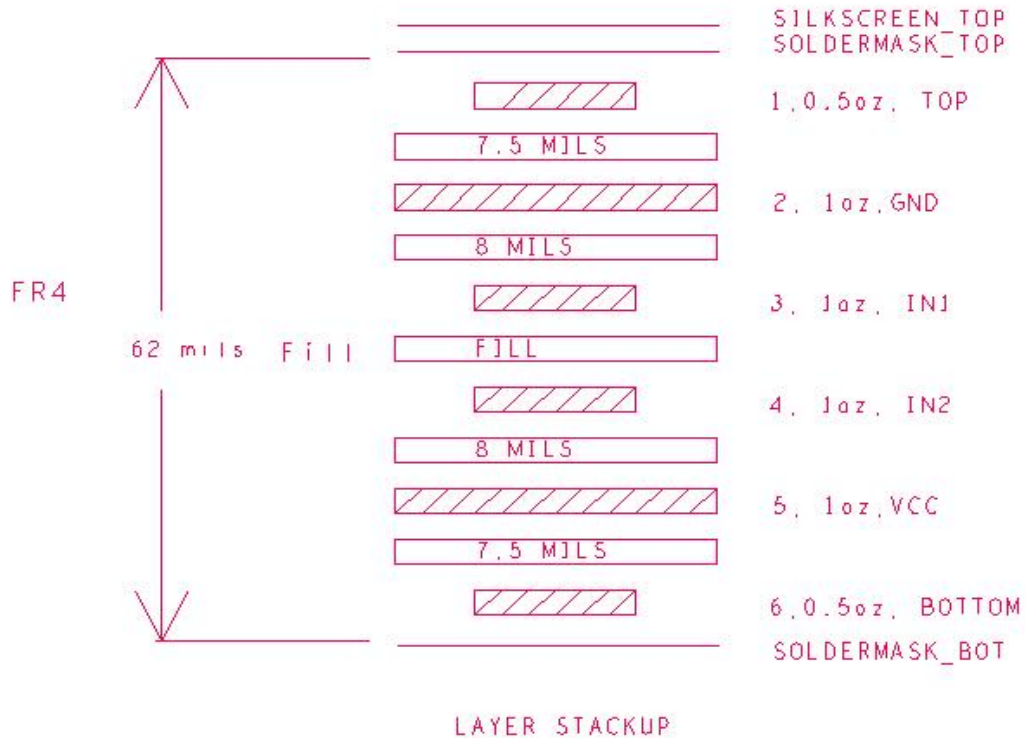


Figure 4 Actual PCB Stackup for the 20050504v02 boards

For impedance calculations, an additional 1/2 oz of plating on the top (signal) copper layer results in a total of 1 oz or approximately 1.4mils thick. Epsilon relative ( $\epsilon_r$ ) for these boards is specified at 4.6.

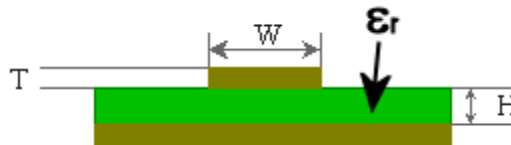


Figure 5 Microstrip Cross Section

A general approximation of single ended (little differential coupling) traces can be used to estimate the unloaded trace impedance.

$$Z_0 = \frac{87}{\sqrt{\epsilon_r + 1.41}} \ln \left( 5.98 \frac{H}{(0.8W + T)} \right) \Omega$$

Figure 6 Single Ended Microstrip

Where: H = Dielectric thickness, T = microstrip thickness, W = microstrip width, and  $\epsilon_r$  is the dielectric constant for the actual PCB material being tested. *Be sure to use the  $\epsilon_r$  that is specified for the TMDS frequency of interest!* Many PCB fabs specify an  $\epsilon_r$  at 1MHz or less which is not necessarily the same for the material at 1.5GHz and beyond.

There are three segments in each of the 4 Mediaguard TMDS pairs can be adjusted to demonstrate the effective increase or decrease in the impedance as needed to offset the package parasitics in the Mediaguard IBIS model. The short segment ( $L_{C-MG}$ ) between the HDMI connector and the Mediaguard chip (Pins 24-35), the segment underneath Mediaguard ( $L_{MG-MG}$ ), and the "stub" segment that leads into the merged differential traces to the HDMI ASIC.

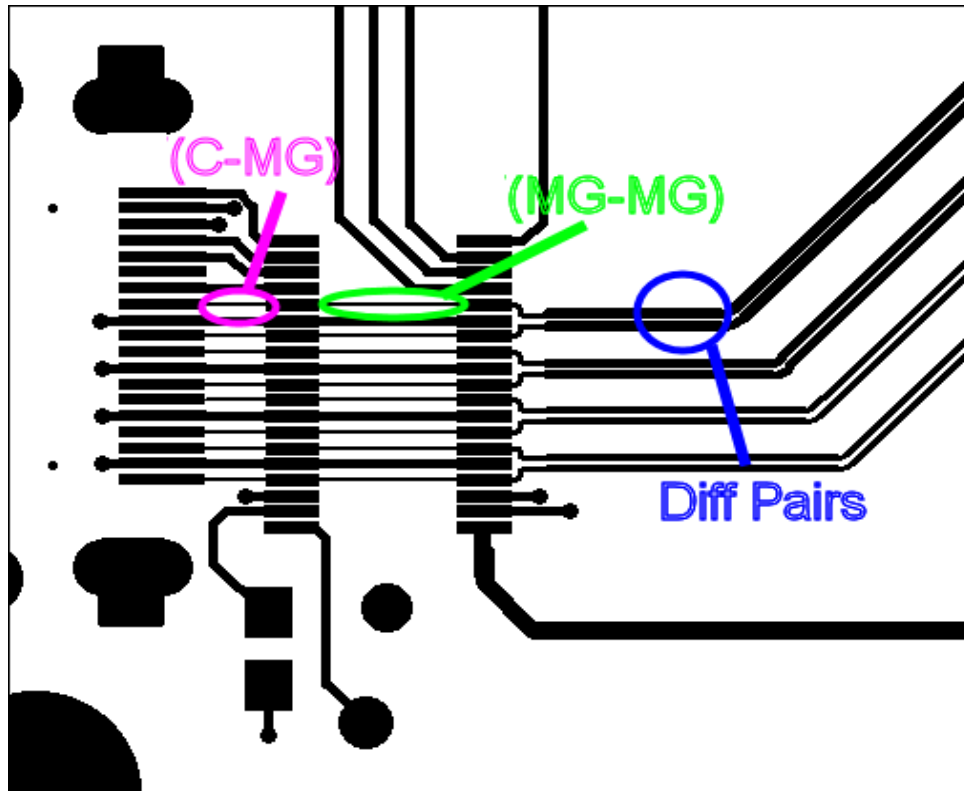


Figure 7 Mediaguard Segment Names

Of each three boards A/D, B/E, and C/F demonstrate 24 possible combinations of layout dimensions on 6 HDMI connectors.

Next is a typical "staggered" layout of the boards.

*Note that each pair is significantly different than adjacent pairs for **comparison** only!! An actual production board would choose a uniform layout for each pair, of course.*

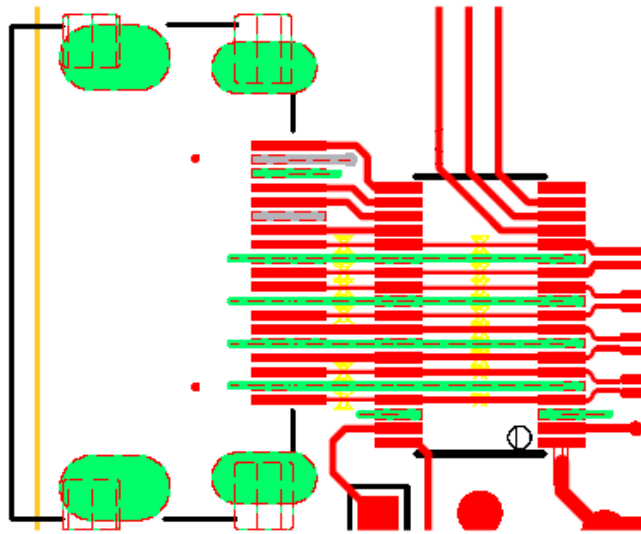


Figure 8 Typical Demo Board "staggered" layout

20050504v02A,D				20050504v02B,E				20050504v02C,F			
	C-MG	MG-MG	STUB		C-MG	MG-MG	STUB		C-MG	MG-MG	STUB
D2	4.5	10	5/8/5	D2	5	10	5/8/5	D2	5.5	10	5/8/5
D1	10	4.5	5/8/5	D1	10	5	5/8/5	D1	10	5.5	5/8/5
D0	4.5	4.5	5/8/5	D0	5	5	5/8/5	D0	5.5	5.5	5/8/5
CK	4.5	4.5	-	CK	5	5	-	CK	5.5	5.5	-

Additionally, each connector's final differential pair is laid out with either 10mil width and 9mil spacing, or 9mil width and 10mil spacing to demonstrate the effect of "lifting" the final tail-out impedance.

Each segment and the final differential pair can individually warp the total impedance measured by TDR. For example, a narrower C-MG segment can raise the impedance of the line just after the connector, while widening the "stub" to the width of the differential pair (as in the TMDS\_CK pairs on these boards) can raise the capacitance and thus lower the impedance as predicted by the general equation:

$$Z_0 = \sqrt{\frac{L}{C}}$$

Figure 9

The following TDR plot has the physical locations associated with the particular impedance inflection labeled.

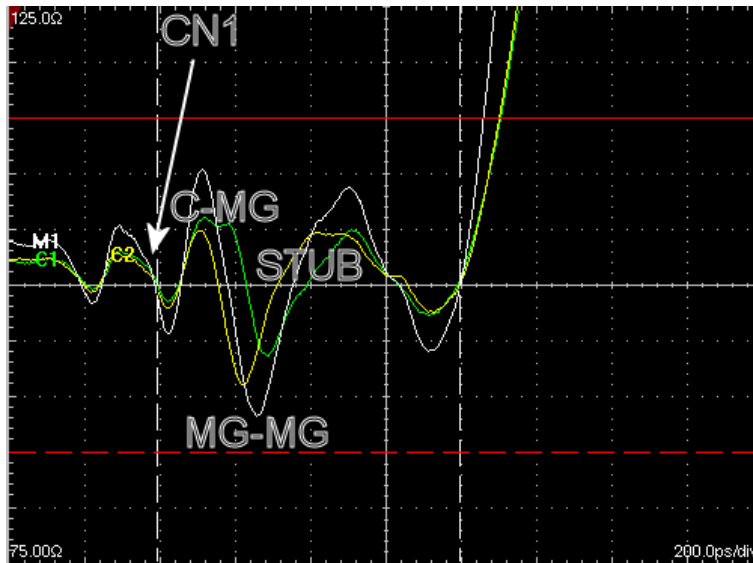


Figure 10 Segment effects on TDR

Figure 10 is a characteristic TDR plot for Board A, CN1, TMDS\_D0. As can be seen from the tables above, the width dimensions of these segments is 4.5mils for C-MG, 4.5mils for MG-MG, and a 5/8/5 stub about 50mils long.

To see the effect of varying the MG-MG width, Figure 8 shows Board A, CN1, TMDS\_D2, where the width dimensions are identical to TMDS\_D0, except that the MG-MG width is more than doubled to 10mils.

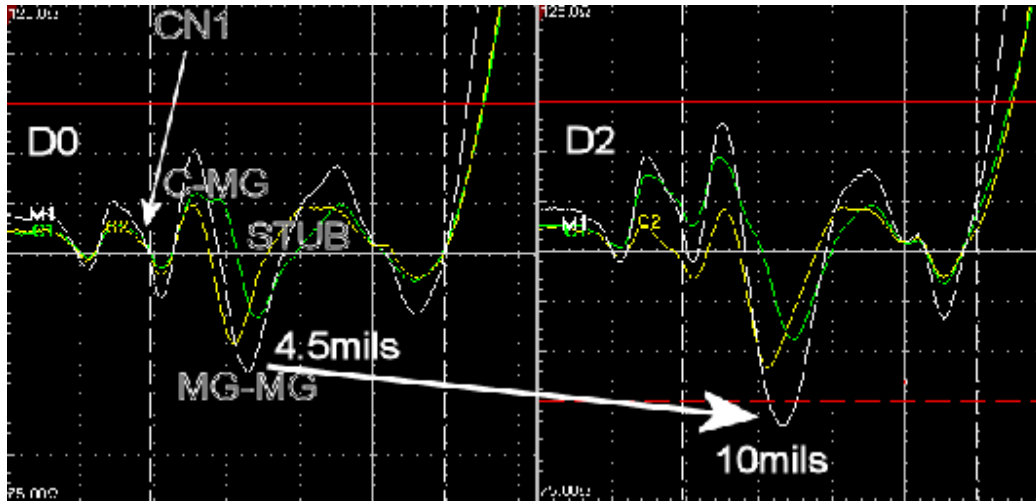


Figure 11 At high resolution (<35ps) individual trace segment adjustments can be discerned.

Also note the "snap back" effect at the C-MG position of the TDR plot. Increasing the MG-MG track width not only increases the capacitance of the MG-MG section, thus lowering the localized impedance, but the widened difference in impedance creates a larger total impedance matching discontinuity between the C-MG and MG-MG segments which pushes the measured TDR spike at the transition even *higher*.

Again, these variances are difficult to discern with the lower resolution of a slower risetime. In Figure 12, the same "failing" traces easily *pass* the HDMI requirements with margin to spare. If there were less margin, it would be more difficult for the designer to determine exactly where to "tweak" the design using 200ps.

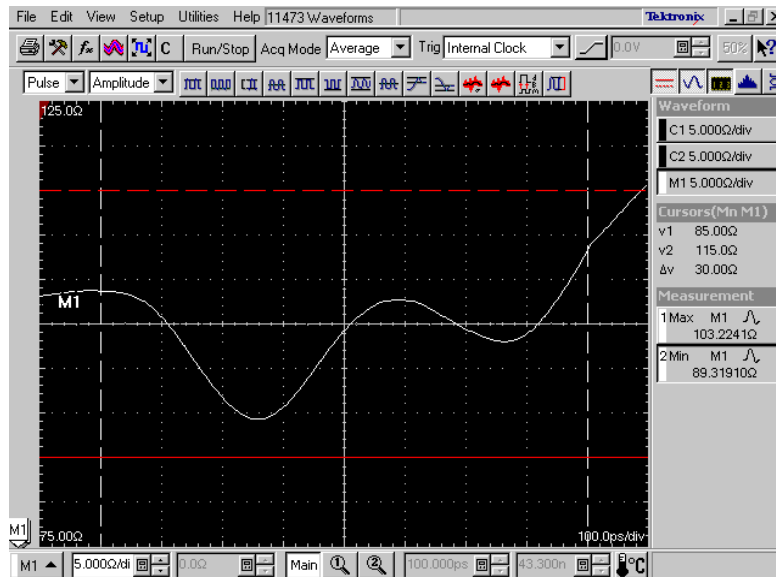


Figure 12 Same traces viewed with 200ps Risetime

This should reinforce the importance of using field solver simulation software for board design, since simple 2D cross sectional calculations/estimations as described above do not account for the overall system interactions. Changing one parameter may have unpredicted effects on simple estimated results.

**TABULAR TDR DATA**

The following Min/Max impedance values have been observed for Boards A, B and C as noted. Boards D, E and F produce similar results except that the termination resistors eliminate the characteristic high-impedance "tail" exhibited by the SiI9031.

***THESE RESULTS ARE TAKEN WITH  $t_r=30ps$ . THEY ARE NOT PASS/FAIL NUMBERS FOR HDMI TESTING.***

BOARD	CONNECTOR	CK MAX	CK MIN	D0 MAX	D0 MIN	D1 MAX	D1 MIN	D2 MAX	D2 MIN
A	CN1	109.5	84.7	108.2	85.4	108.1	84.9	110.8	80.6
A	CN2	109.6	84	107.8	85.6	104.6	84.4	110.3	81.4
B	CN3	108.2	83.5	109.5	86.7	107	84.3	111.3	81
B	CN4	108.5	83.1	109.6	87.4	104.1	83.4	111.7	82
C	CN5	107	82.2	110.3	87.9	106.1	82.7	112.2	81.7
C	CN6	107.1	81.6	110.3	88.2	103.4	82.6	112.9	82.8

**DESIGNING A SUCCESSFUL SYSTEM**

Adding MediaGuard™ interface protection to your HDMI port design obviously enhances ESD and backdrive/isolation protection for the system, but it can also enhance signal integrity in a correctly designed system.

A few general steps should be followed for each design.

- 1. Gather design info. Get Stackup data and  $\epsilon_r$  for the target PCB fab process (6 layer, 4 layer, etc.) Review CMD Application documents.**
- 2. Design rough layout. Identify HDMI connector location and HDMI ASIC location. Minimize the C-MG traces and route them straight through. Remove tight bends and sharp corners in traces.**
- 3. Consult field solver software for the unloaded traces, and factor in the IBIS models of parasitics for Mediaguard.**
- 4. Review each TMDS pair's layout individually. Mediaguard provides industry leading closely matched parasitics for minimized inter- and intra-pair skew, however the typical variances described in the IBIS model should be reviewed on each of the 8 traces.**
- 5. Take advantage of CMD's design review services. Contact Applications Engineering for assistance.**
- 6. After building prototypes, take advantage of CMD's TDR lab facilities.**

***REMEMBER: These principles apply with or without MediaGuard! HDMI requires controlled impedance layout techniques described here whether or not protection devices are used!***



**REFERENCES**

"CONTROLLED IMPEDANCE AND TIME DOMAIN REFLECTOMETRY (TDR)", 1996,  
<http://www.thetestlab.com/data/sep96.pdf>, Bob Neves, Microtek Labs

"Design Guidelines for Electronic Packaging Utilizing High-Speed Techniques ", IPC D-317A, 1995, Institute for Interconnecting and Packaging Electronic Circuits

"High-Definition Multimedia Interface Compliance Test Specification", 2003, Version 1.0a

**SOFTWARE RESOURCES**

<http://www.ansoft.com/> - Maxwell 2D/3D

<http://www.cadence.com/> - Spectraquest

<http://www.mentor.com/> - Hyperlynx

<http://www.polarinstruments.com/> - Si8000 Solver

<http://www.apsimtech.com/> - RLGC

**PLEASE REVIEW ALL OF THE CURRENT DESIGN GUIDELINES AVAILABLE AT**

<http://www.calmicro.com/applications/customer/downloads/current-cmd-mediaguard-design-guidelines.zip>

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