AP-220 Low-Capacitance ESD protection on High-Speed Ports (USB 2.0 and DVI)

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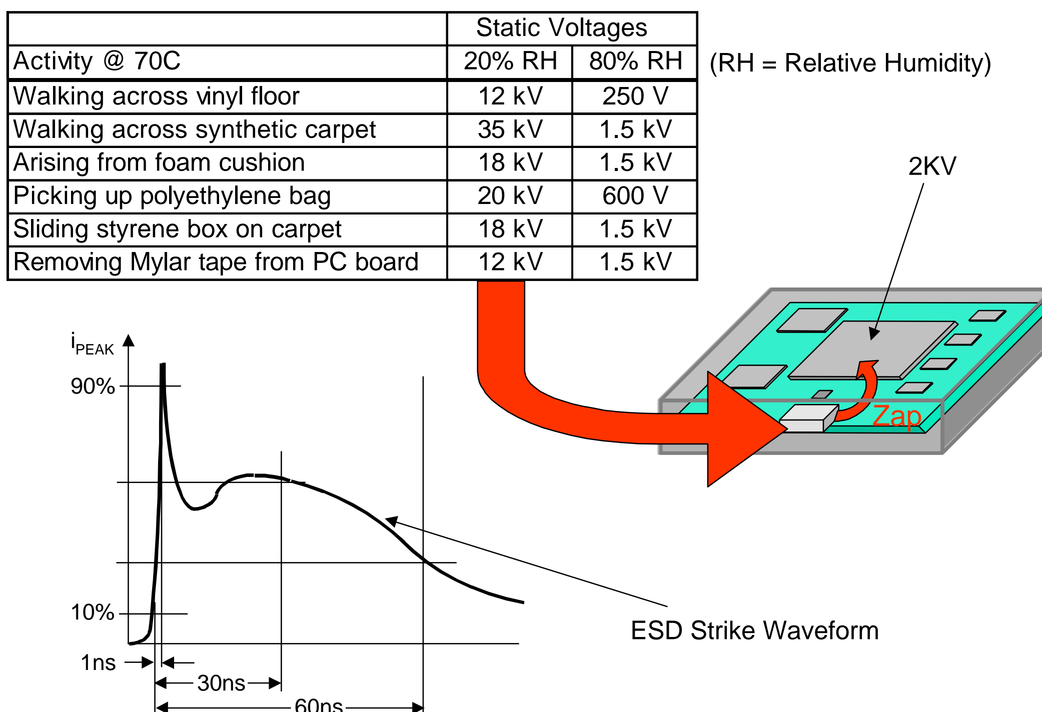
The Need for ESD Protection

High speed interfaces such as USB2.0, DVI and its derivative HDMI are now being used extensively in the computer and consumer markets. The USB2.0 interface comprises one pair of differential digital signals at data rates up to 480Mbps, and is used for connection to peripherals in PCs, notebooks, embedded computers and workstations. The DVI interface comprises either 4 or 7 differential pairs of digital signals at around 165Mbps, and is used in some notebooks to connect to the new LCD flat panel displays, and as the HMDI interface in new TVs, DVRs, and set top boxes.

These ports are subject to human contact such by as someone touching any of the pins on the connector, or any of the pins on an open-ended cable connected to one of the ports. As a result, these ports are likely to experience ESD strikes that can destroy the internal expensive systems ICs causing an equipment return, and therefore they need ESD protection to protect these ICs. However, these ports transfer data at high speed between two devices, requiring that the port at each end have very low capacitive loading, so that the signals on each line do not get distorted. Fortunately new low cost devices are now available that both protect against ESD yet do not capacitively load the signals.

ESD protection is needed because it is relatively easy for a user to send an electrostatic discharge through one of the connector pins to the I/O pins of the expensive systems chip, and is therefore important to protect. These CMOS devices often have some degree of internal ESD protection included, typically from 1KV to 2KV of protection. Although this level of protection is satisfactory for handling in a manufacturing environment where strict ESD abatement controls are enforced, it is inadequate for general end-user handling. Figure 1 shows that by just doing normal everyday actions, ESD discharges can damage the systems chip.



	Static Voltages	
Activity @ 70C	20% RH	80% RH
Walking across vinyl floor	12 kV	250 V
Walking across synthetic carpet	35 kV	1.5 kV
Arising from foam cushion	18 kV	1.5 kV
Picking up polyethylene bag	20 kV	600 V
Sliding styrene box on carpet	18 kV	1.5 kV
Removing Mylar tape from PC board	12 kV	1.5 kV

Figure 1. Normal everyday activities can cause ESD at high enough voltages to cause permanent damage to the main digital ICs that usually only protect to 2KV (HBM)

In relatively dry environments electrostatic discharge voltages can be a lot higher than the protection levels offered by any systems IC, so if an ESD strike gets through to the systems chip, it is likely to destroy its I/O circuitry inside the chip. Designers of computers and consumer equipment must allow for use in such dry environments, such as during long summers or in desert type areas. As an example, a user in a relatively dry environment may walk across a synthetic carpet to connect a PC to a USB2.0 disk drive, or a flat panel display with DVI, connecting the PC first. This leaves the other end of the cable exposed, so if the user then touches any of the free connector's pins, an electrostatic discharge will pass through the USB cable to the PC, straight to the systems chip. If the ESD strike is severe enough, parts of the chip will be permanently damaged.

There are two popular standards for testing of ESD protection devices: the HBM (Human Body Model); and the much tougher-to-meet IEC 61000-4-2 now used worldwide. The IEC standard requires the tester to apply a pulse of about 60ns, with a waveform as shown in Figure 1, through a 330ohm resistor and a 150pF capacitor, producing a peak current of over 25A for a 8KV discharge. [For more information refer to Figure 11 in the Appendix.] This current discharges into the ESD protector, but without the ESD protector, the entire current pulse will have to be absorbed by the systems chip.

These systems chips are expensive. Also the geometries of the gates are continually becoming smaller, making them ever more susceptible to ESD damage. At the same time PCs are becoming more and more popular in the home because of the graphics capabilities for games, so there is a likelihood that kids may play around with cables and connectors, making the chances of an ESD strike reasonably likely during the lifetime of the equipment. Computer and consumer equipment designers must design for this scenario.

There are two approaches that designers can take to protect against ESD strikes. One is mechanical and the other electrical. For example, any path that allows the discharge to quickly go to ground (thereby bypassing the susceptible IC) is a benefit. This can be through the connector shield, or the ground plane on the PCB, or it can be through a device that absorbs the discharge or diverts it quickly to ground, or all of the above, as shown in Figure 2.

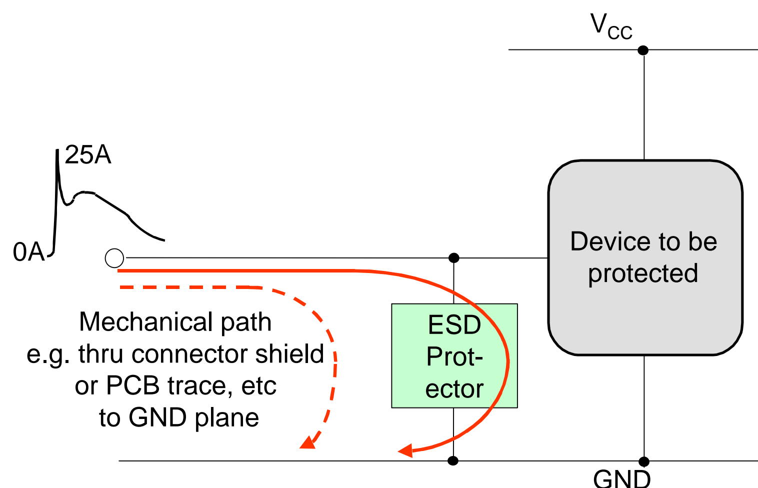


Figure 2. ESD Strike takes any path to GND

So if an ESD protecion device can withstand 8KV contact discharge, correctly designed equipment will be able to withstand a much bigger strike. Computer and consumer manufacturers test their equipment to the IEC standard, and typically this is 8KV contact discharge, although some new consumer equipment is tested to 15KV or higher. Also after each ESD strike the equipment should not deteriorate in its ability to withstand more strikes.

Although some designers make great efforts to eliminate the need for additional devices on the board by using just mechanical means, it is much more economical to also use an ESD protection device for safety reasons. Having to return a computer that has a blown systems chip is inconvenient to the user and expensive for the manufacturer. It is a question of cost – is it cheaper to accept a percentage of returned products, or to add a protection component by the connector? Manufacturers of computers, notebooks, TVs and set top boxes have to determine whether it is worth adding ESD protection devices costing around $0.20. Anything worse than 1 in 500 returns makes it uneconimical to omit an ESD protection device.

There are a number of protection devices readily available that can protect against ESD, but there can be issues with them in high-speed applications that make them unusable. This is because the data rates are 480Mbps for USB2.0, and around 165Mbps or higher for DVI. At these data rates, any small amount of capacitance on the whole link from the systems chip through the connectors and cable to the peripheral can sufficiently distort the signal that the digital information can be altered. The total parasitic capacitance can be minimized by using low capacitance ESD protection devices.

These devices should be inserted close to the connector at each end of the cable: both in the computer and in the peripheral. This is because the ESD strike will be immediately absorbed by the ESD protector before it can get to the sensitive ICs downstream. An ESD strike is most likely to occur when the user is linking the two devices together. Depending on which one is connected first will make that equipment more susceptible, because the pins at the end of the cable can be touched sending an ESD strike down the cable, through the connector, to the systems IC. With ESD protectors in both the computer and peripheral, the total unwanted capacitance is twice the capacitance value of each ESD protector.

A number of ESD protection devices can address the problem of ESD strikes, but each has disadvantages. [A more detailed analysis of ESD protection devices is in the Appendix.]

Varistors do protect against ESD strikes but their capability to sustain repeated strikes is not good. This is because the breakdown voltage of varistors weakens after each strike: refer to individual manufacturers data sheets. A problem with polymer devices is that the trigger voltage is fairly high, such that smaller strikes may not trigger the varistor causing the whole discharge to go into the systems IC. If the strike lasts a sufficiently long time, permanent damage may occur on the systems IC. Varistors and polymers have been used for first generation high-speed interfaces but are now being replaced by more predictable and reliable ESD protection diodes.

There are two main types of ESD protection diode: a zener diode; and a dual rail clamp diode structure. The zener diode is connected between the signal line and ground. A negative strike will cause the zener to act as a forward biased diode that starts conducting when the voltage across it exceeds around 0.6V. A positive ESD strike will cause the zener to go into breakdown and start conducting when the voltage across it exceeds around 6.5V. In either case the zener diode absorbs the bulk of the strike energy and the systems IC is protected. The big disadvantage of the zener approach is that the capacitance from the channel I/O pin to ground is typically 20pF to 100pF. Although zeners are popular ESD protectors at lower data rates, this capacitance on the signal line is far too high for the higher data rates.

An alternate approach for ESD protection devices is to use dual rail clamp diodes instead, as shown in Figure 3.

ESD Protection for High Speed Interfaces

Dual rail clamp diodes have a capacitance from input to Ground of from 1pF to 7pF, making them better suited to high-speed signals. With the dual rail clamp, a negative ESD strike on the I/O pin will cause the lower diode to forward bias, thereby transferring the discharge through the lower diode into ground. A positive ESD strike on the I/O pin will cause the upper diode to forward bias causing the discharge to transfer its energy to the V_{CC} rail. For maximum protection, the

discharge must dissipate into ground. So there must be a good discharge path from V_{CC} through to ground for the systems IC to be adequately protected. This means that either there must be a good high-speed ceramic capacitor (with low equivalent series resistance and inductance) or a zener diode from V_{CC} to ground placed close by, as shown in the lower part of Figure 3. Although the dual rail clamp types of protection device may need more additional components than a zener diode, their capacitive loading on the line is adequate for high speed data. But because typically there are two such devices on the line, one in the host and one in the

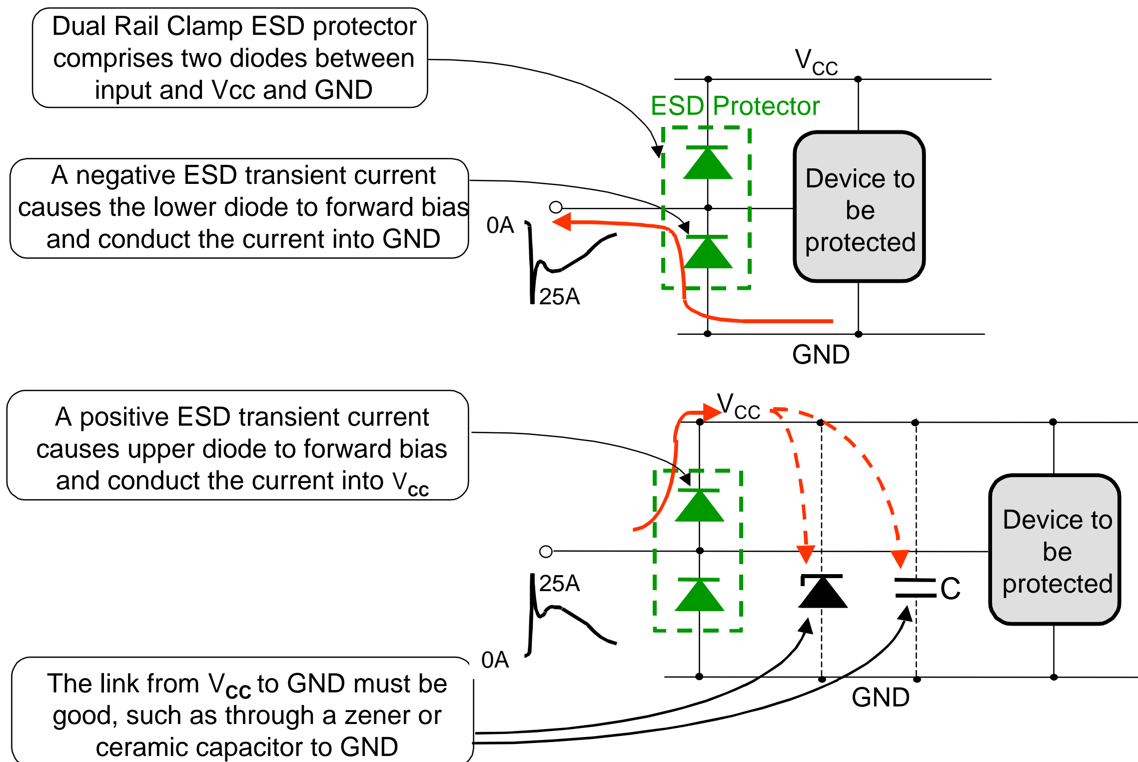


Figure 3. Dual Rail Clamp Diodes Protect against ESD Strikes of Either Polarity

peripheral, this doubles the capacitive loading. So the lower the capacitance of the protection device, the lower the overall capacitance and the less errors there will be.

The effect of line input capacitance C_{IN} is shown in Figure 4, which shows the digital waveform becoming distorted. Obviously the larger C_{IN}, the more distorted the signal becomes, and the more errors will occur. Another important factor that can affect performance is the matching capacitance ΔC_{IN} between one I/O pin and another. This is particularly important for differential signal transmission, because the signal lines are driven by matching drivers with matching receivers at the other end. So it is important that the I/O to GND capacitance on the pins is also matched.

Figure 4 also highlights another problem – capacitive-coupled cross-talk between the lines. This can be caused by adjacent trace capacitance, or by channel I/O to I/O capacitance C_{CH} on the ESD diode. This is even more important for USB2.0 and DVI, where the clock and data signals are differential and cross-talk becomes a crucial factor and therefore has to be minimized.

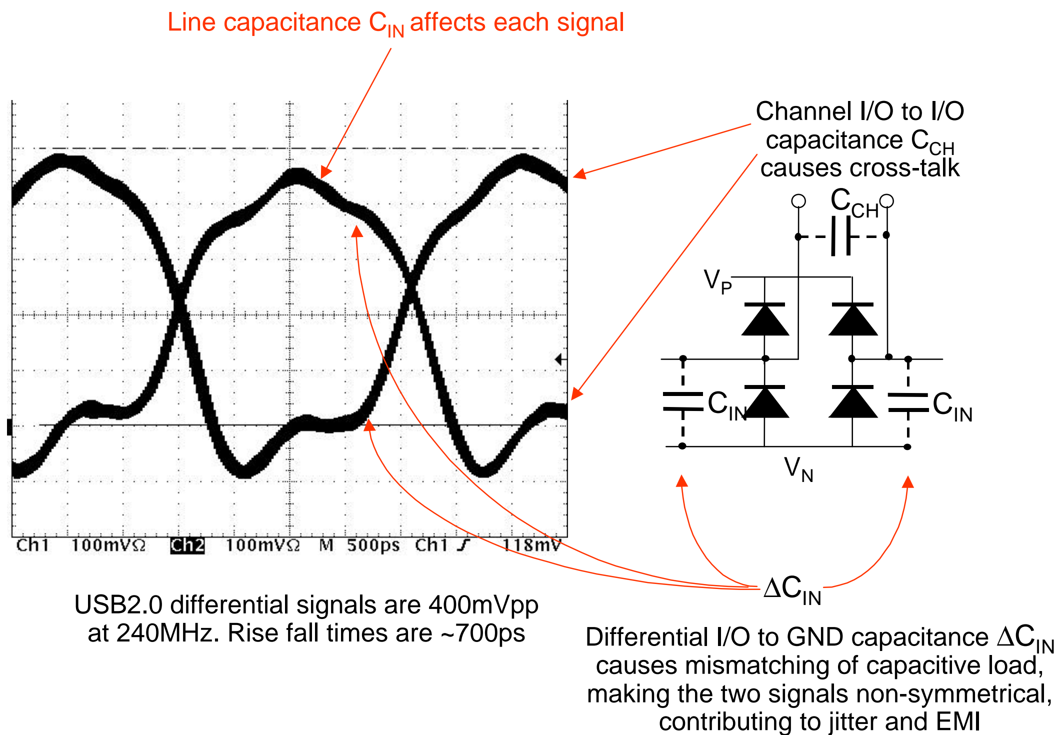


Figure 4. The Need for Low Capacitance ESD Protection Devices for High Speed Signals

The total capacitance budget includes the two connectors, the cable, the traces on each of the two PCBs, and the I/O capacitance of the two ICs involved – the systems IC and the peripheral IC, as well as the ESD protection diodes, as shown in Figure 5.

Introducing the CM1213 Family

Fortunately California Micro Devices new CM1213 ESD protection family has been introduced that simultaneously solves two problems: low capacitance; and the need for additional components. The CM1213 has three features relevant to low capacitance: a low input capacitance C_{IN} of 1pF (I/O to GND), a very small channel I/O to GND capacitance difference ΔC_{IN} between inputs of 0.02pF, and a low channel I/O to I/O capacitance C_{CH} of 0.8pF. It also has an embedded zener diode from V_{CC} to ground, alleviating the need in most design layouts for an external by-pass capacitor to transfer the discharge to ground. Another advantage is that the max ESD rating is 8KV contact discharge, meeting the stringent requirements of the international standard for ESD protection, IEC61000-4-2 level 4. The CM1213 is offered in 1-channel, 2-channel, 4-channel, 6-channel and 8-channel versions. The SOT23-packaged versions of the original CM1210 introduced in 2002 are pin-compatible with the CM1213.

So for USB2.0 with a signal at 480Mbps, this corresponds to a fundamental frequency of 240MHz, and noticeable (but decreasing magnitude) odd harmonics of 720MHz, 1.2GHz, and 1.68GHz. A 1pF value for capacitor C_{IN} in Figure 5 will have an impedance of approximately 660ohms, 220ohms, 132ohms and 94ohms respectively. With a line driver source impedance of 45ohm, this is reasonable, but for a 3pF capacitance the impedances become 220ohms, 73ohms, 44ohms and 31ohms. These latter values are closer to the source impedance and will affect the ‘eye’ pattern. Also the 1pF capacitor will contribute less than 100ps to the 700ps rise / fall times,

whereas a 3pF capacitor will contribute a lot more. But it is more the difference in line capacitance ΔC_{IN} that counts rather than each absolute value.

Capacitance loading = [Driver + Receiver + Trace + ESD + Connector] * 2 + Cable

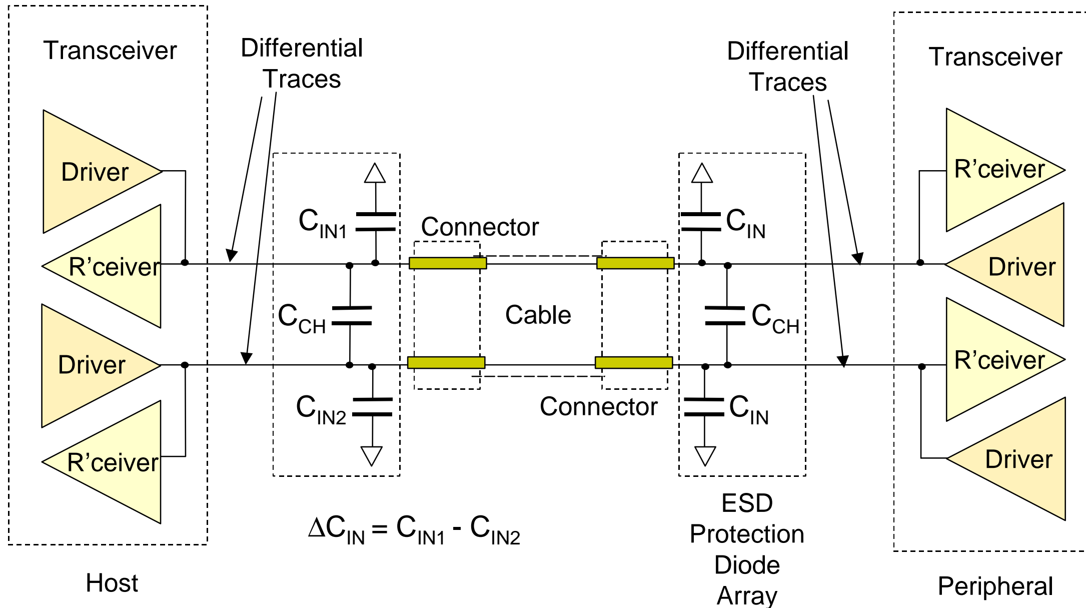


Figure 5. Differential Signals and Capacitive Loading

The differential I/O to GND capacitance of the CM1213 is 0.02pF, so the effect on the difference in the waveforms can basically be ignored because it is so small. If it was larger, as with most ESD protection devices, or very large for standard diode pairs in a single chip, then there would be a non-symmetrical difference in the two signals. This would contribute to jitter thereby increasing the error rate, depending on all the other parameters affecting the signal. There may also be an increase in EMI which may force better filtering.

All of these features make the CSM1213 family ideal for USB2.0 and DVI / HDMI.

The USB 2.0 Interface

USB2.0 has now replaced USB1.1 on all new computers as well as many new peripherals, and the issue of capacitive loading on the differential signal lines is a serious problem. For USB1.1, ESD protection devices having moderate capacitances could be used to shunt the ESD current away from the systems ICs without distorting the 1.5Mbps or 12Mbps signals. With the much higher 480Mbps speed of USB Version 2.0, a minuscule capacitance will distort the signals beyond the specification. [For more detailed information on USB2.0 and its component specifications, refer to the Appendix.]

This section covers the requirements of USB 2.0 and how systems ICs can be protected against ESD damage while still enabling 480Mbps operation, although there are no definitive ESD specifications in the USB 2.0 Standard. The USB 2.0 standard does not specify the high-speed capacitance requirements in the same way as for USB1.1. The only capacitance requirements

stated are for the transceiver die and package. The standard requires that the capacitance of the signal lines of the transceiver chip, as an isolated component, have a capacitance to ground of 10pF or less with D+ and D- matching within 1.0pF. The limits on the delay of the signal going from the transceiver to the connector are monitored using differential Time Delay Reflectometer (TDR) measurements.

The “High Speed USB Platform Design Guidelines” published by Intel provide several rules of thumb for high speed USB signal layouts, which can greatly affect the impedance matching and signal integrity. These guidelines along with the constraints of the physical board can determine the most desirable packaging and layout for a given application, some of which are shown in Figure 6.

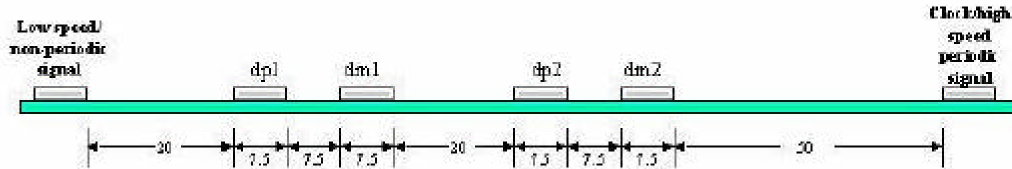


Figure 6. Intel’s recommendation for PSB trace widths and spacing

For a 63 mil thick 2s2p PCB with 1 oz copper:

7.5 mil traces spaced 7.5 mils apart yields approximately a 90Ω transmission line
Maintain 20 mil spacing minimum to other signals and other USB pairs
Maintain 50 mil spacing minimum to high speed periodic signals (clocks, etc.)
Maintain <150 mils total mismatch between D+ and D- pair lengths
Avoid stubs for component attach, but if necessary, keep them to <200 mils long

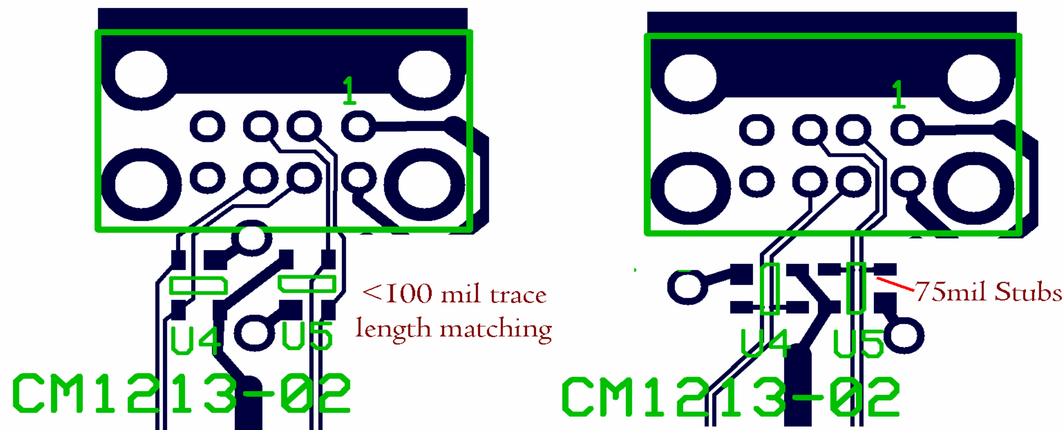


Figure 7. USB2.0 Layout with CM1213-02 ESD Protectors

For a single USB 2.0 port, the CM1213-02 integrates two pairs of diodes for protecting the two differential signal lines into a SOT143-4 package. The layout in Figure 7 shows dual CM1213-02’s with a stacked Dual Type A connector for two USB 2.0 ports. Orienting the protection devices “perpendicular” to the signal traces (left) provides the smoothest transition from transmission line to protection device pad. However, by orienting the devices in-line with the signal traces, and providing very short stub traces (right) the minimum disruption of the matched transmission line can be achieved while still staying within the Intel Recommended Layout Guidelines.

The DVI Interface

The Digital Visual Interface specification from the Digital Display Working Group (DDWG) has standardized the means for clocking pixel data discretely to the monitor or flat panel display. CRT displays provide an essentially continuous row of pixels which are scanned by a constant velocity electron beam, thereby tracing as many pixels onto a screen as the bandwidth of the RGB signals will allow. Plasma and LCD displays, however, have discrete pixel grids which must match exactly with the X-Y image driven from the video graphics chip. Many of these discrete grid displays include Digital-to-Analog frame conversion logic to synchronize standard analog VGA RGB signals to the LCD / Plasma X-Y grid. Even a very small timing difference between the graphics chip and the frame recapture logic can seriously deteriorate and alias the image quality, as the pixelated image content is interpolated to "fit" the fixed X-Y grid.

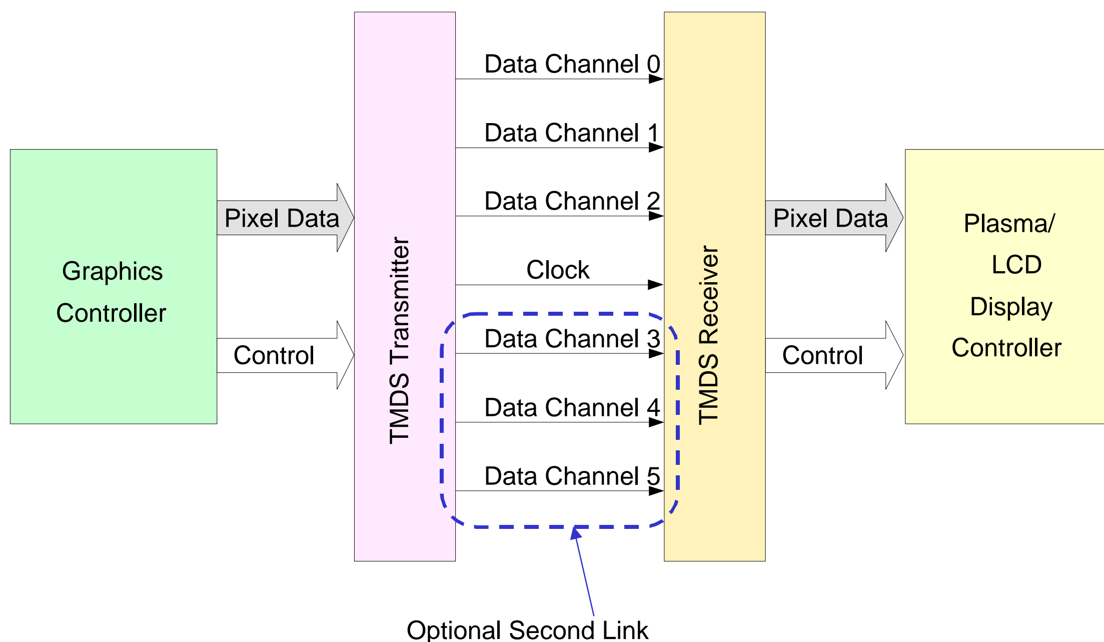


Figure 8. DVI Interface

The DVI interface provides a standard method to transfer encoded digital pixel data synchronized to a master clock which can be used in LCD and Plasma displays to eliminate this aliasing and image degradation. The encoding scheme uses "Transition Minimized Differential Signaling," or TMDS, across 4 or 7 differential pairs, see Figure 8.
DVI adds the additional protection challenge of limiting digital clock/data skew, above and beyond the inherent bandwidth and loading issues of high frequency VGA signals. Data Channels 3 through 5 are optional, and may be populated in some applications, and omitted in other lower cost designs. When both sets of channels are used, odd pixel data are encoded on Channels 0-2, and even pixel data are encoded on Channels 3-5.

This creates a potential difficulty for protection device partitioning from the 26-pin DVI connector. The Single Channel TMDS configuration requires 4 differential signals (Clock + Channels 0-2), or 8 lines to be protected. The Dual Channel TMDS configuration requires an additional 6 lines of protection for Channels 3-5.

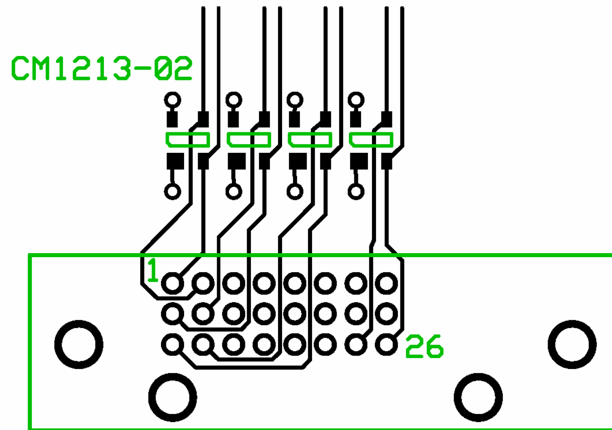


Figure 9. Layout of four 2-channel CM1213s to the DVI Connector

Using discrete protection devices of any type can cause imbalances in differential loading, since parasitic load can vary substantially, sometimes by even more than their tolerances for specified characteristics. Figure 9 shows a sample layout for a Single Channel DVI connector with four CM1213-02's. By utilizing one CM1213-02 dual channel device on each differential pair, the designer can guarantee the close load matching between each (+) and (-) signal, since the dual devices are fabricated on the same silicon die.

Alternatively, to provide the maximum channel-to-channel matching, a CM1213-08 can be used as shown in Figure 10.

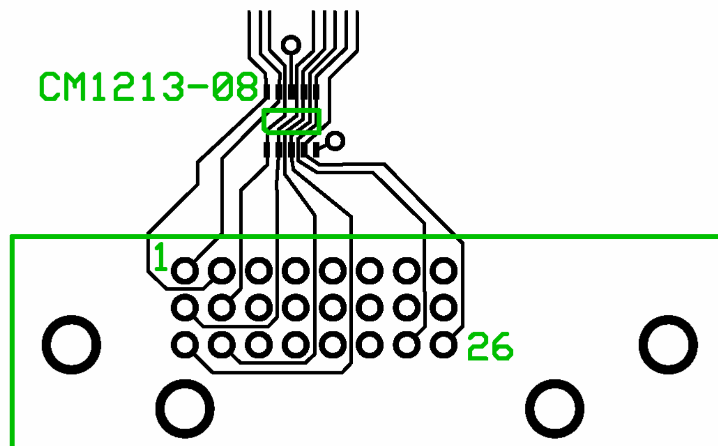


Figure 10. Layout of 8-channel CM1213-08 to the DVI Connector

Finally, a combination of -08 and/or -02 packages can be used to protect a Dual Channel DVI port. The combination low clamping voltages, high kV breakdown voltage, low parasitic load and close port-to-port matching makes the CM1213 ideal for DVI port protection.

Appendix

ESD Requirements

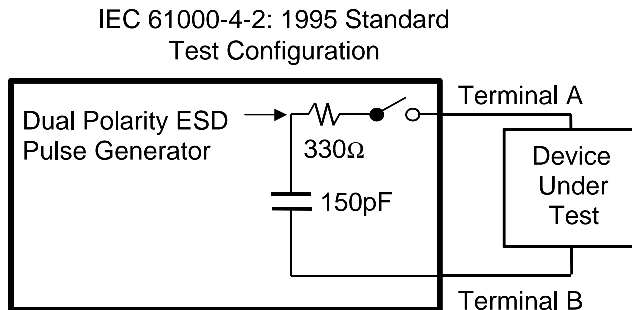
To achieve operation at higher data rates of over 200Mbps, systems IC manufacturers have had to decrease the minimum dimensions of the transistors, interconnections, and the SiO_2 insulation layers. This results in smaller structures that are more susceptible to damage at lower energy levels than when the IC geometries were larger. Also SiO_2 layers are more likely to rupture and metal traces are more likely to open or bridge, all of which is increasing ESD vulnerability. To compound the problem, there is a proliferation of laptop computers being used in uncontrolled environments (i.e. no wrist grounding straps or conductive/grounded table surfaces) where people are likely to touch connector pins during the connecting and disconnecting of cables.

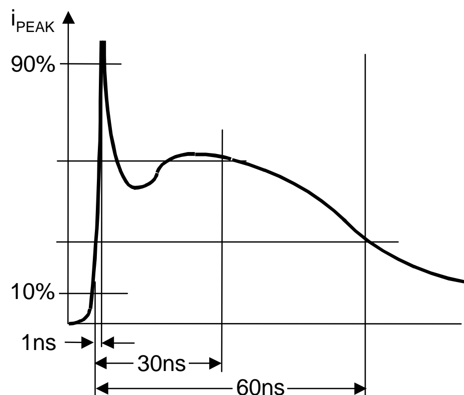
Traditional methods to shunt ESD energy away from the systems ICs used zener diodes and MOVs (Metal Oxide Varistors) with moderate capacitances of 10pF to 100pF. With the higher data rate interfaces, these devices distort the signal beyond recognition / detection.

Some systems ICs are designed with limited internal ESD protection allowing them to tolerate from 1KV to 2KV pulses (per the Human Body Model), but some ICs are not capable of tolerating even 100V without suffering damage. Many IC data sheets do not specify an ESD tolerance voltage; so the user may have to test to learn what the tolerance is.

To enable uniform testing of devices for ESD tolerance, there are two popular standards: the HBM (Human Body Model) which came from the USA MIL-STD-883, and the more stringent IEC61000-4-2, now used worldwide. The IEC standard shown in Figure 11 requires the tester to store a charge 50% larger than the HBM and to discharge it through a resistor that is about one-fifth the size of the HBM one, resulting in a much shorter pulse rise time and a peak current many times larger. The highest direct-contact-to-the-pins ESD voltage of the IEC standard is 8KV which has become something of a defacto industry standard. A 8KV Level 4 peak signal into a 330Ω resistor is in effect a 25A peak current into either the systems IC or into the ESD protection device. Both standards use a prescribed pulse waveform that testers must duplicate.

IEC 61000-4-2: 1995 Standard
Test Configuration





- Fast discharge from 150pF capacitor through 330Ω resistor
- 6 ESD pulses
  - 3 positive, 3 negative
  - 1 second apart
- “Contact” *vs.* “Air” discharge
  - Different levels
  - Usually contact discharge is the crucial parameter

Figure 11. IEC 61000-4-2: 1995 Standard

ESD Protection Device Types

Zener Diodes

Zener diode protectors have about 30 pF of capacitance which is too high to successfully pass 480MHz signals without significant distortion, which would result in unreliable detection of USB2.0 signals. Zener diodes could be made with lower capacitances but may result in ESD voltages insufficient to meet the 8kV protection levels necessary.

TVS Diodes

There are some Transient Voltage Suppressor (TVS) devices on the market that add a regular diode in series with the zener diode to effectively lower the net capacitance. To handle positive and negative polarity ESD pulses, a second Zener and series diode pair of the opposite polarity needs to be in put in parallel with the first pair of diodes. Unfortunately the resulting capacitance of 5-6pF is still not low enough to avoid distortion of high data rate signals.

MOVs (Metal Oxide Varistors)

MOVs can have lower capacitances than the TVS devices, but currently the lowest capacitance MOV device available has a capacitance of 3.0pF which contributes too much capacitance for high data rate signals.

Polymer Devices

Polymers devices have resistances that are voltage dependent. With a low voltage, e.g. 5V, the impedance is in the Giga ohm realm. When a high voltage is applied across the polymer device, the resistance drops to a very low value so that tens of Amperes can be shunted to ground. These polymers are good for high frequency applications because of their low capacitance of 0.05pF to 1.0pF. But polymers have some not-so-attractive side effects. Unlike zener diodes which breakdown at the same voltage that they clamp to, the polymer does not breakdown until it reaches a voltage that is much higher than the final clamping voltage. Figure 12 shows how a typical polymer breaks down at up to 1KV, then it snaps back to a clamping voltage of up to 150V. After the charge is dissipated, the polymer returns to its high impedance state.

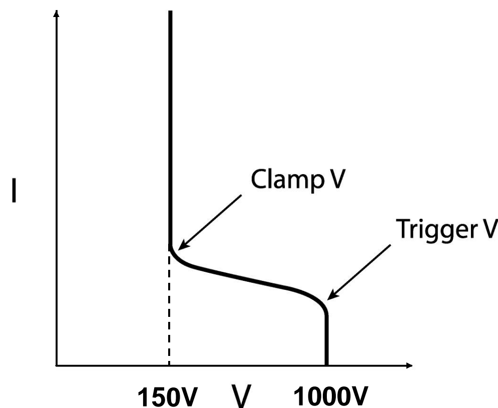


Figure 12. Polymer response to high voltage strike

Consequently these polymer devices can be used only in applications where the systems ICs have their own built-in ESD protection and can tolerate the “trigger” voltage of the polymer device (trigger voltages vary from 300V to 1000V, clamping voltages vary from 60V to 150V). Polymers are fairly new on the market and their data sheets are filled with “typical” specifications without guaranteed minimums / maximums. Also graphs on some of the polymer data sheets show that the specifications degrade based on the number of ESD pulses they receive. Data sheets only guarantee the specifications over a lifetime of a limited number of ESD pulses, which can be as low as 20 pulses.

Dual Rail Clamp Diodes
Regular diodes can be used to clamp the ESD pulses to the power or ground rail so that the current flow is always in the diode's forward direction.This permits the use of smaller and therefore lower capacitance diodes than used for zeners. Positive ESD pulses are clamped to V_{BUS} (+5V) and negative ESD pulses are clamped to GND. Some users implement this scheme with standard low-capacitance diodes. These diodes are cheap, readily available, and have a capacitance of 1.5pF per diode (so the capacitance on the signal is 3.0pF for the two diodes), which is too high for high data rate signals. But even worse, they were not designed for high current ESD pulses and have no specifications that guarantee their use with the high currents and voltages of ESD pulses, or with repetitive high-current ESD pulses. Some will degrade and eventually fail at the high ESD voltage and currents.

There are also integrated configurations for multiple data channels provided by California Micro Devices and others that have about 3pF capacitance for the two diodes and which have been designed for repetitive high-voltage, high-current ESD pulses.

Correct Placement of ESD Protectors

Because of the nature of ESD strikes, it is vitally important to place ESD protectors correctly both with regards to the ESD source (usually a connector) and the systems chip to be protected. So any ESD protector requires careful circuit design and layout. While the total ESD energy is not too high, the current waveforms can ramp from zero to ten's of Amperes in a nanosecond. Such massive di/dt makes the application extremely sensitive to parasitic inductances. This is because a large voltage drop can occur across a very small inductance since V = L di/dt. Figure 13 shows an ESD protector in a typical application, with a right way and wrong way to connect.

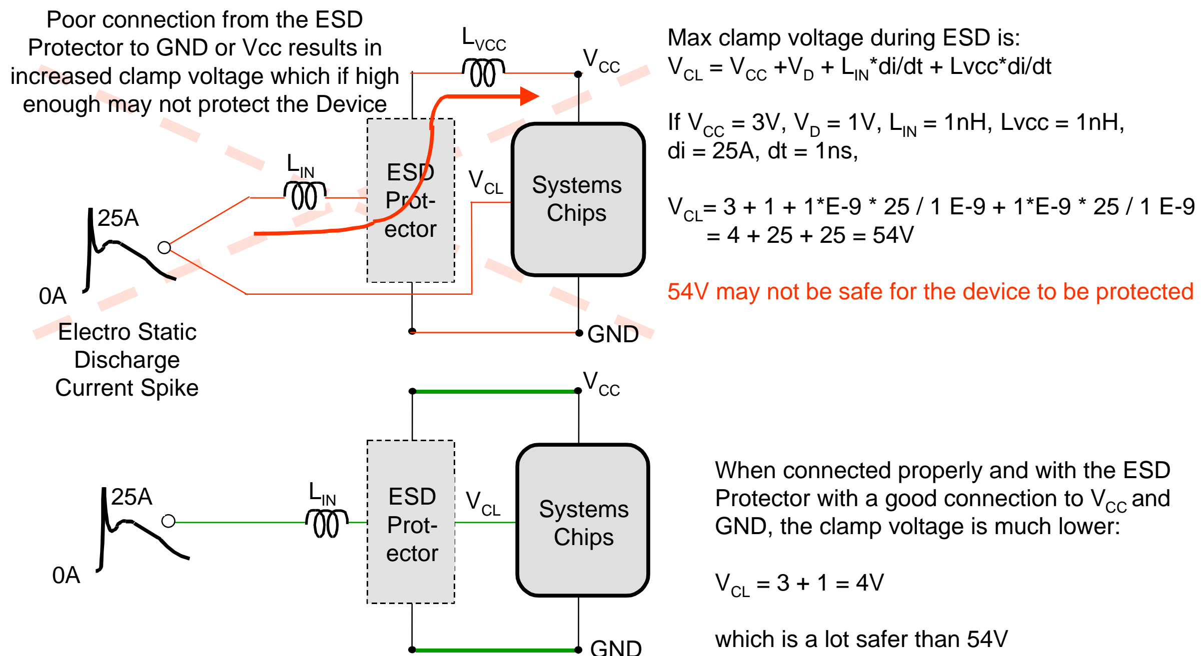


Figure 13. Beware of Poor Trace Links to ESD Protectors and Systems Chips

The top portion of Figure 13 shows two parasitic inductances, LIN and LVCC. LIN is the equivalent inductance from the connector along a stub to the ESD protector, including the connector pin and the trace inductance. It shows that stubs must be kept to a minimum. Depending on the PCB material etc, about 1cm of trace is about 1nH, so the closer the ESD protector is to the connector the better, especially if there is a branch trace as shown with a long stub to the protection device. If not, and say a 1nH inductance is between the connector pin and the ESD protector I/O pin, then the 1ns edge of the ESD strike creates a sizable voltage across the inductor. For example, if the ESD strike is 8KV peak, a 0 to 25A peak current will flow through 1nH in 1ns causing a 25V peak voltage across the inductance.

This means that although the ESD protector limits the I/O voltage to its clamping voltage, the voltage on the systems IC will be the clampng voltage plus the voltage across the inductance of 25V. This will be an even higher voltage if there is an inductance from the connector pin to the systems IC pin (not shown). Also if there is another inductance of say 1nH from the Vp rail of the ESD protector to Vcc as shown, then in the case of a positive strike, the voltage across this inductance will also be added to the supply rail voltage, the clamp voltage, and the first inductance voltage. So the total voltage at the systems IC pin could easily be 54V. This may or may not be OK, but it is much safer to connect the ESD protector as shown in the lower portion of Figure 13, where the trace goes straight through the protector's pin to the systems IC, such that there is no stub. The voltage on the systems IC is the same as the protector. The left-hand layout of Figure 7 is a good example of such a connection, although the right hand layout is still reasonable with 75mil stubs, because this represents less than 0.1nH.

Figure 14 is a more detailed analysis and shows all the traces represented by parasitic inductances that might arise from poor layout configurations.

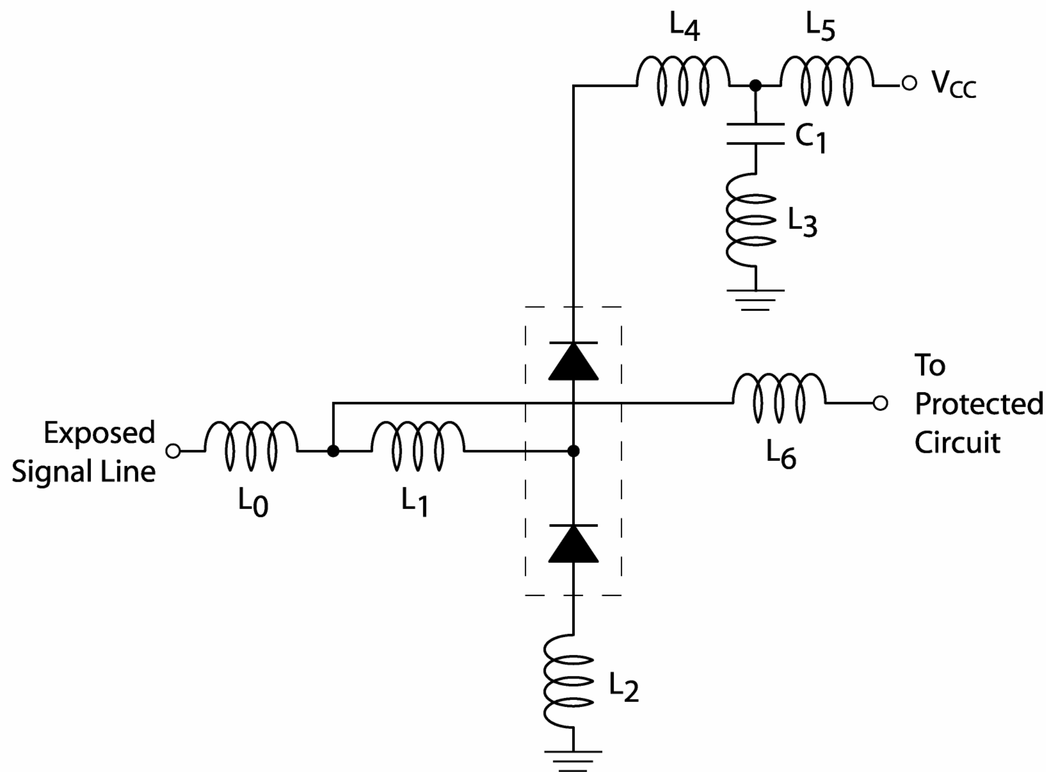


Figure 14. Possible Parasitic Inductances in the PCB Traces

The effects of these parasitics are:

1) **Inductors L_0, L_1 and L_6:** Inductors L_0 and L_6 represent the signal line necessary to get from the connector to the internal electronics. L_1 is the inductance of the stub when the ESD protection device is connected to the main signal line via a stub. This inductance should be minimized and avoided whenever possible, as it allows a higher voltage level to be transmitted to the critical device until the Back-EMF of L_1 can be overcome. Ideally, the signal line should go directly from the external connector to the ESD protection device and from there to the internal electronics with no stubs involved. Also, it is usually best to place the ESD protection device close to the connector, minimizing L_0, and leaving whatever signal line that is required to get inside the system to act as inductor L_6, to shield the internal devices. This also keeps the high ESD voltages and electromagnetic fields created by the ESD current away from other signal lines in the system to avoid possible arcing or cross coupling, i.e. Electromagnetic Interference (EMI).
2) **L_5:** Inductor L_5 represents the inductance from the power pin of the ESD protection circuit to the power supply and to additional bypass capacitors (not shown) that could be used to absorb more of the ESD pulse energy in addition to a by-pass capacitor. This connection to the power supply should always be as direct and as low impedance as possible.
3) **C_1:** Bypass capacitor C_1 should be added to absorb most of the positive ESD pulse when a zener diode is not integrated in the ESD protection device, such as with the CM1210. The CM1213 does have an embedded zener and if there is a good trace link to Vcc, there should be no need for the capacitor. If there is a need for a capacitor, it should be large enough to absorb the ESD current without the local supply voltage being significantly increased, typically a ceramic 0.1uF.
4) **L_3 and L_4:** Inductor L_4 represents the interconnections between the ESD protection device and the bypass capacitor, and L_3 from the bypass capacitor to a good ground plane. If these inductances are not small, they will limit the effectiveness of the diode clamp during positive ESD pulses. The lines must be short and wide and C_1 should have its ground side tied directly to the ground plane.
5) **L_2:** Inductor L_2 represents the interconnection from the negative-pulse ESD protection diode to the ground plane. As in the other cases, this line must be as short and as wide as possible to minimize the inductance.

ESD Protection for USB 2.0 Systems

ESD protection is needed for the USB host and hub, although there are no definitive ESD specifications in the USB 2.0 Standard. Instead, the USB standard directs developers to apply accepted industry practices and regulatory agency standards for ESD/EMI. In addition, on Intel's website, the "High Speed USB Platform Design Guidelines" is available with a section on ESD protection.

The power pins in the cable are V_{BUS} = 5V and GND = 0V. A host or hub port must supply 500mA or 100mA of current. The "high-speed" signals on the D+ and D- signal lines swing between zero and 400mV at 480 Mps. The data encoding scheme is NRZI so the signal frequency is always equal to or lower than the data bit rate, so the maximum frequency is 480MHz. The USB2.0 host uses an initial handshake to learn and adapt to the maximum speed of each peripheral.

High speed USB cables contain two signal and two power wires, and are required to have shields and twisted pair signal conductors. The standard does not specify a cable capacitance, and no cable manufacturer specifies a capacitance. Instead, the standard specifies the cable's differential characteristic impedance at 90Ω ±15%, which is the same as the output impedance of two drivers with each driver's Zout = 45Ω and the PCB's impedance of the differential-signal traces. The cable's common mode characteristic impedance is specified at 30Ω ±30%, and the driver's output impedance to GND is specified at 45Ω. This non-specification of capacitance is

done because at 480Mbps the cable is a transmission line with a characteristic impedance, and can not be treated as a lumped capacitance.

The length is limited by maximum specifications of the propagation delay and signal-pair attenuation. The maximum one-way delay for high speed cable is 26ns, the PCB traces on a downstream port on a host or hub can add 3ns, and the traces on the upstream port on a hub or peripheral can add 1ns from cable to transceiver. The traces on the PCB must have the same 90Ω differential characteristic impedance as the cable. The USB2.0 Standard also contains a table of maximum allowable cable loss versus frequency (although the table only goes up to 400MHz and not 480MHz): the maximum allowable attenuation for a cable at 400MHz is 5.8dB. for up to 5 meter long cables.

The standard allows the USB connector to have no more than 2.0pF capacitance. The power pins on the connector are required to be longer than the signal pins so they contact first to enable hot-plugging. The downstream ports of hosts or hubs have type-A receptacles which are rectangular shape with in-line pins, and the upstream ports of hubs and peripherals have type-B receptacles which are square shape with two rows of pins.

For transceiver and trace capacitance, and propagation times at 480Mbps, the USB2.0 standard does not specify the high-speed capacitance requirements the same as for full and low-speeds. The only capacitance requirements stated are that the transceiver die and package have a capacitance to ground of 10pF or less with D+ and D- matching within 1.0pF. The limits on the delay of the signal going from the transceiver to the connector are monitored using differential Time Delay Reflectometer (TDR) measurements. These measurements are defined in section 7.1.6.2 of the USB 2.0 Standard as:

- The following specifications must be met with the incident rise time of the differential TDR set to 400ps. It is important to note that all times are “as displayed” on the TDR and are hence “round trip times.” Termination Impedance (Z_{HSTERM}) is measured on the TDR trace at a specific measurement time following the connector reference time. The connector reference time is determined by disconnecting the TDR connection from the port connector and noting the time of the open circuit step. For an A connector, the measurement time is 8ns after the connector reference location. For a B connector, the measurement time is 4ns after the connector reference location. The differential termination impedance must be: $80\Omega \leq Z_{HSTERM} \leq 100\Omega$. Through Impedance ($Z_{HSTHRU}$) is the impedance measured from 500ps before the connector reference location until the time governed by the Termination impedance specification [$70\Omega \leq Z_{HSTHRU} \leq 110\Omega$]. In the Exception Window (a sliding 1.4ns window inside the Through Impedance time window), the differential impedance may exceed the Through limits. No single excursion, however, may exceed the Through limits for more than twice the TDR rise time (400ps).