

Dual-Port HDMI Sink Application with Integrated I²C Multiplexing

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INTRODUCTION

The following schematic in Figure 1 describes the general architecture of a typical dual-port HDMI Sink design. For simplification, CEC is not implemented in these schematics, since there are multiple methods of aggregating CEC ports. This is covered separately.

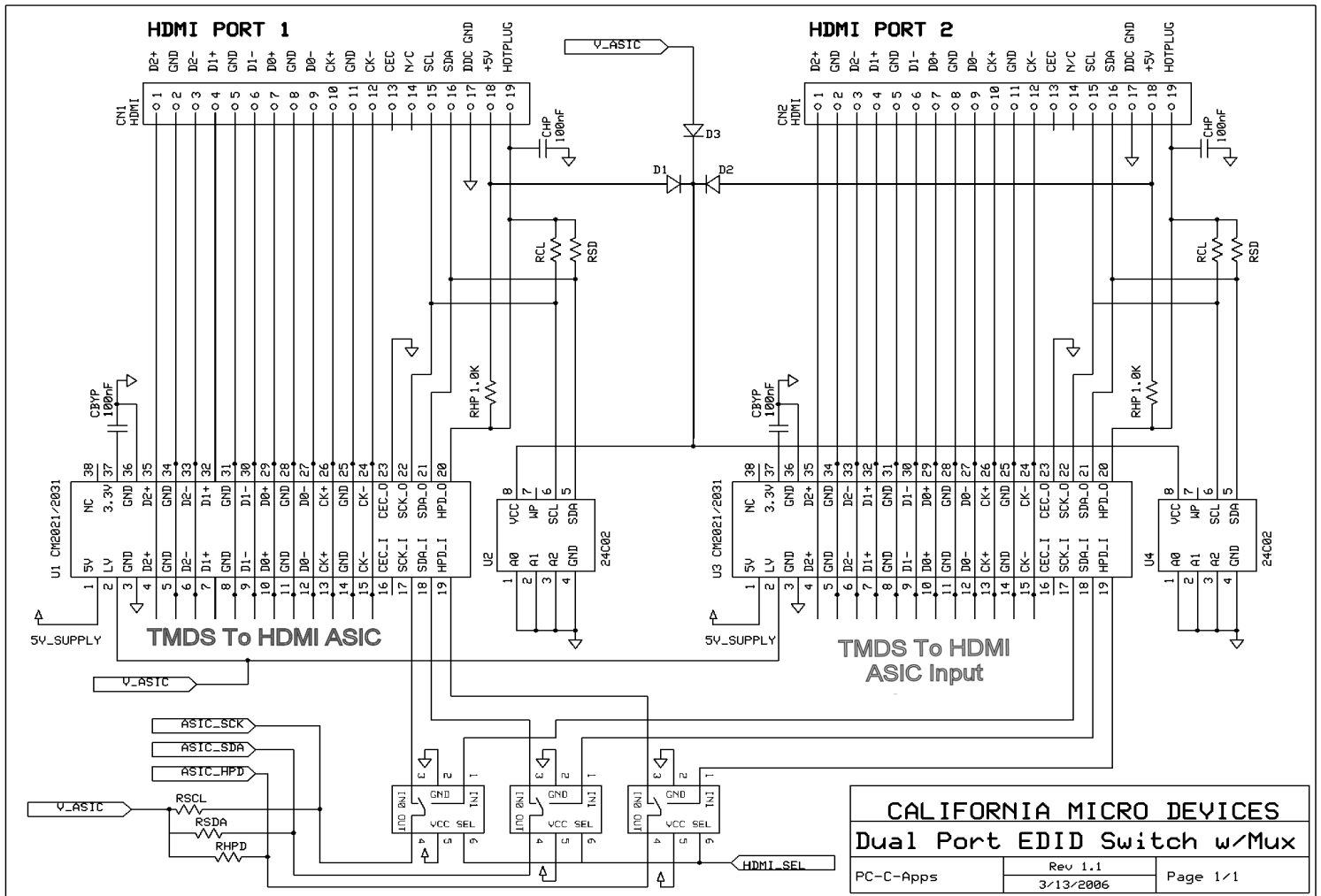


Figure 1- Typical Dual Port HDMI Application

The system in Figure 1 uses three (3) discrete 2:1 Mux chips to switch local microcontroller I²C access to both EEPROM ports. The third mux chip also allows microcontroller control of each individual HotPlug line as discussed below.

Section 8.5 of the HDMI Specification allows the HDMI Sink to pulse the HotPlug line "low" for at least 100msec to indicate to the Source that the EEPROM should be re-read. This function can be implemented with a few discrete components as shown in Figure 2.

The Hot Plug Detect circuit of the CM2021 is specifically designed to provide this "pulse" capability. The bi-directional logic can also allow monitoring of the status of the port by tri-stating the GPIO, and monitor the voltage on HDMI Connector Pin 19.

Finally, by creatively switching the LV_SUPPLY bias current, multiple CM2021 devices can be paralleled to create an N:1 multiplexer for the 4 low speed bi-directional circuits. When LV_SUPPLY is driven low, the SCL, SDA, CEC, and HPD circuits enter isolation mode and go hi-Z. (See Figure 3)

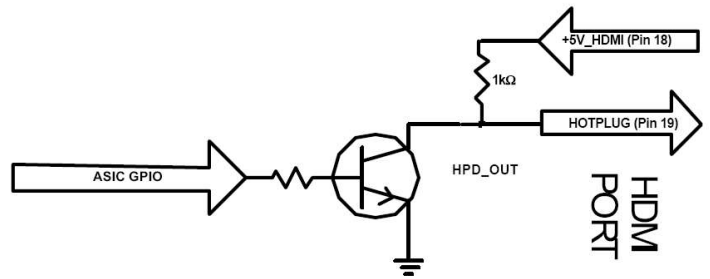


Figure 2- Typical Discrete Implementation of a Shunt Pulsing Circuit for HPD Reset

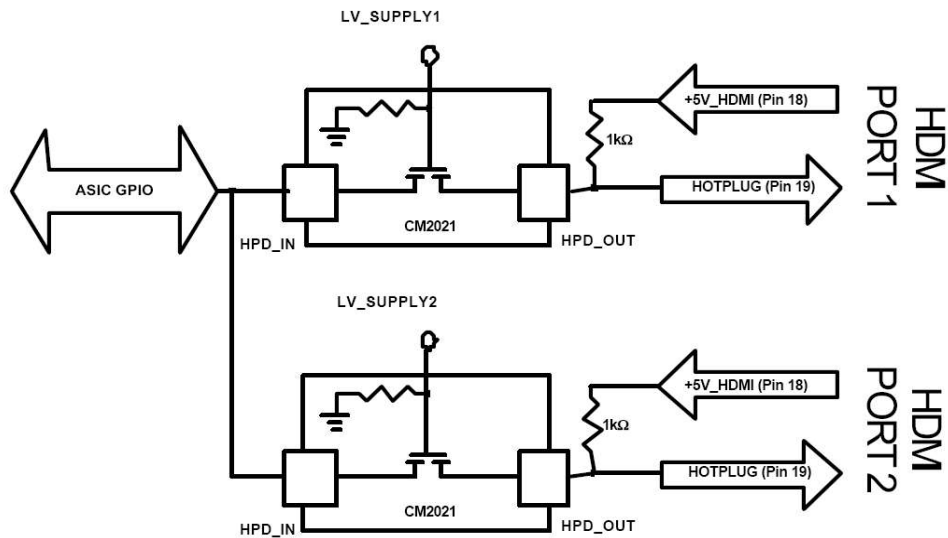
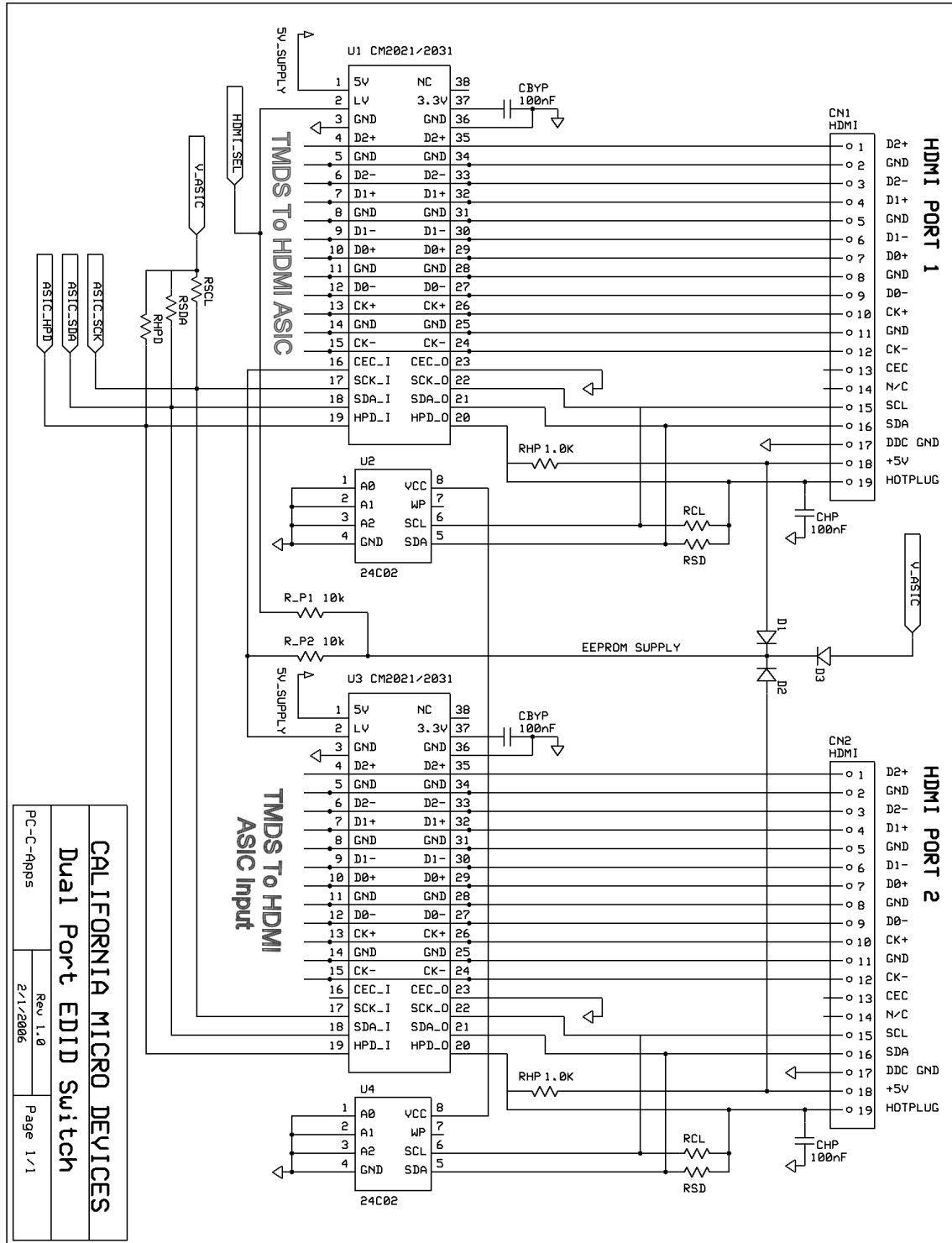


Figure 3- Hot Plug Detect Switching, Pulsing, and Monitoring with CM2021

Figure 3 shows the circuit savings and simplicity of using the CM2021 to provide this function and more.

By further extending the use of the CM2021 internal FETs, the discrete N:1 Mux chips may also be eliminated as shown in Figure 4. This "distributed mux" design allows large numbers of HDMI Ports in multiple geographic PCB locations without the need for routing all SDA/SCL/HPD lines to a single multiplexer. They may be "daisy chained" throughout the system with a single set of traces for routing simplicity.



CALIFORNIA MICRO DEVICES
Dual Port EDID Switch
PC-C-Alpps
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Figure 4- Eliminating need for discrete I2C 2:1 mux chips



If independent GPIO's are used to bias, or "switch" the LV_SUPPLY's of each CM2021, then each EEPROM/Port can be switched independently by a 1-of-N decode circuit. If (as in Figure 4) the CEC circuitry is not used, then it can be reused to provide the decode function and reduce the control to a single "High/Low" input signal (HDMI_SEL) without any additional components.

Here, the unused CEC FETs are used to "switch" the CM2021 level shifter blocks as follows:

- **When HDMI_SEL is "high"**, then U1 LV_SUPPLY is biased high, or "on," (this requires only a few hundred microamps provided through R_P1.)
When Port 1's U1 LV_SUPPLY is high, then ASIC_SCK, ASIC_SDA, and ASIC_HPD can control Port 1's EEPROM and HPD line. First, the local microcontroller drives ASIC_HPD low (to inhibit HPD on the source**), and then the microcontroller has complete access to Port 1's EEPROM via ASIC_SCK and ASIC_SDA.
Also, when U1 LV_SUPPLY is "high", then the unused CEC level shifter is enabled, which passes through the "low" from the GND level applied on Pin 23 to Pin 16. This pulls R_P2 "low" which disables the Level Shifters on Port 2's U3. This effectively isolates Port 2's EEPROM and HPD switching logic from ASIC_SCK, ASIC_SDA, and ASIC_HPD.
The external HDMI Source may then access the Port 2 EEPROM without affecting Port 1 or the local microcontroller.
- **When HDMI_SEL is "low"**, then R_P1 is pulled down, and U1 LV_SUPPLY is biased low, or "off". This effectively isolates Port 1's EEPROM and HPD switching logic from ASIC_SCK, ASIC_SDA, and ASIC_HPD.
When U1 LV_SUPPLY is "low/off", then the unused CEC level shifter is disabled, which *isolates* the "low" from the GND level applied on Pin 23, and Pin 16 is pulled "high" by R_P2, which brings U3's LV_SUPPLY "high," or "on". (this requires only a few hundred microamps provided through R_P2.)
When Port 2's U3 LV_SUPPLY is high, then ASIC_SCK, ASIC_SDA, and ASIC_HPD can control Port 2's EEPROM and HPD line. As with Port 1, the local microcontroller simply drives ASIC_HPD low (to inhibit HPD on the source**), and then the microcontroller has complete access to Port 2's EEPROM via ASIC_SCK and ASIC_SDA.
The external HDMI Source may then access the Port 1 EEPROM without affecting Port 2 or the local microcontroller.
- **When NEITHER Port Access is required by the microcontroller**, then all three lines (ASIC_SCK, ASIC_SDA, and ASIC_HPD) are merely driven "high" and both CM2021's will provide isolation through the normal operation of the level shifter. As an additional feature, each port may still be monitored, or "listened to" by polling HDMI_SEL. When HDMI_SEL is "high," the microcontroller may use its I/OD input to detect a high or low on ASIC_HPD to determine if an active Source is connected to Port 1. When HDMI_SEL is "low," the microcontroller may use its I/OD input to detect a high or low on ASIC_HPD to determine if an active Source is connected to Port 2.

** This is the Hot Plug switching function mentioned in Section 8.5 of the HDMI Specification.

LAYOUT ISSUES

Each HDMI Port should be laid out as usual with the MediaGuard device laid out as close as possible to the connector as shown in Figure 5.

**PLEASE REVIEW ALL OF THE CURRENT HDMI DESIGN GUIDELINES AVAILABLE AT
<http://www.calmicro.com/applications/customer/downloads/current-cmd-mediaguard-design-guidelines.zip>
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OTHER APPLICATION NOTE REFERENCES

<http://www.calmicro.com/applications/customer/downloads/200500707-Mediaguard-Comparative-Impedance-Boards.pdf>
<http://www.calmicro.com/applications/customer/downloads/20051218-mediaguard-impedance-comparison-thin-dielectrics.pdf>
<http://www.calmicro.com/applications/customer/downloads/20050529-MG-EEPROM-Options.pdf>

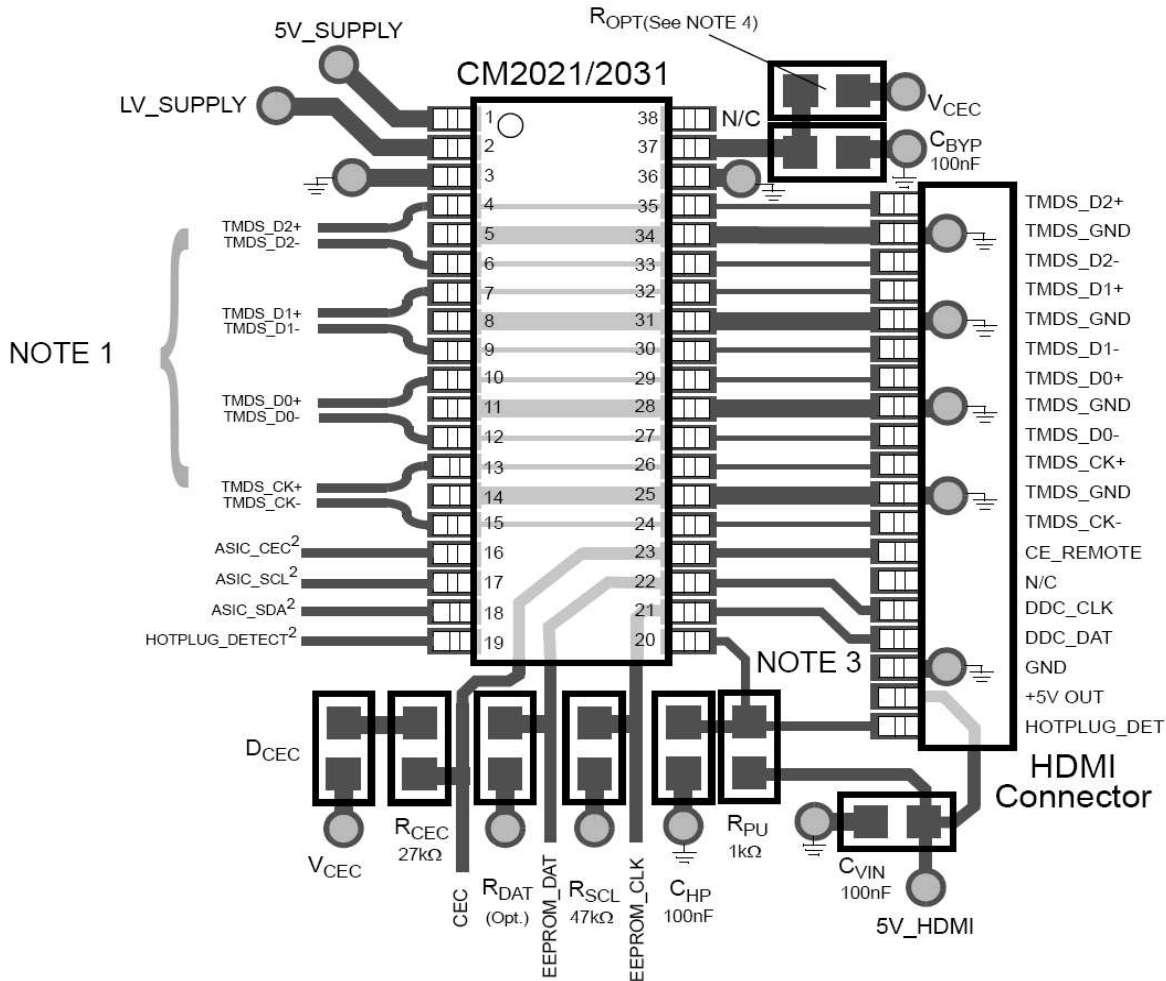


Figure 5- Typical Single Port Layout

¹ Differential TMDS Pairs should be designed as normal 100Ω HDMI Microstrip. *Single Ended (decoupled) TMDS traces underneath MediaGuard™, and traces between MediaGuard™ and Connector should be tuned to match chip/connector IBIS parasitics. (See MediaGuard™ Layout Application Notes.)*

² Level Shifter signals should be biased with a weak pullup to the desired local LV_SUPPLY. If the local ASIC includes sufficient pullups to register a logic high, then external pullups may not be needed.

³ Place MediaGuard™ as close to the connector as possible, and as with any controlled impedance line always avoid placing any silkscreen printing over TMDS traces.

⁴ CM2021/CM2031 footprint compatibility. For the CM2031, Pin 37 becomes the V_CEC power supply pin for the slew-rate limiting circuitry. This can be supplied by a 0Ω jumper to V_CEC which should be depopulated to utilize the CM2021. The 100nF C_BYN is recommended for all applications.

⁵ CEC pullup isolation. The 27k R_CEC and a Schottky D_CEC provide required isolation for the CEC pullup.